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Generic Complex Programmable Logic Device (CPLD) Board

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Abstract: **The design and development of Generic Complex Programmable Logic Device (CPLD) Board is to emphasis on the reduction of the overall design & development life cycle time of the products. Since the Programmable Logic Devices are very flexible, reconfigurable, the same board can be utilised in multiple system designs. These devices work at very low voltage, high speed and low power consumption. These features make the PLDs more versatile and increase the product reliability to the greater extent as the device count at the system level reduces enormously. Present board has on board Joint Testing Action Group (JTAG) interfaces for In-System programming purpose. This makes the board to be more flexible, in terms of design changes, up gradation and easy migration from one specification to another. The generic nature of the present work is demonstrated by implementing A5/1 Algorithm, Seven segment display driver, Binary counter, LED control logic and so on.**

Key Words: **CPLD, Development Cycle, JTAG, PLD, Flexible, Migration, Low power, Binary counter, Algorithm, High Speed.**

1. INTRODUCTION

The need to respond to the changing scenario of the market standards in a compressed time to market window has led the wide spread use of programmable logic devices (PLDs) in a broad range of applications such as telecom infrastructure, consumer electronics, industrial and medical fields. Power supply sequencing, voltage and current monitoring, bus bridging, voltage level translation, interface control, and temperature measurement are typical board functions found in these applications**.** System designers are faced with continual pressure to meet their development schedules, and need to implement designs with minimal effort and risk while maintaining maximum flexibility. By using a programmable-based approach instead of several discrete devices or Application Specific Standard Products (ASSPs), designers can accelerate their time-to market, address system cost, space reduction, and ensure a high level of product differentiation [1].

Programmable Logic Devices (PLDs) are a critical component in embedded industrial designs. PLDs have evolved in industrial designs from providing simple glue logic, to the use of FPGAs as a coprocessor. This technique allows for I/O expansion and off loads the primary microcontroller (MCU) or digital signal processor (DSP) device in applications such as communications, motor control, I/O modules, and image processing [2].

It is shown and proved that the PWM technique is widely used in most of the industrial power controls. The developments of high frequency PWM generator architecture for power converter control using FPGA/ CPLD ICs are more versatile and easy to implement. The resulting PWM frequency depends on the target FPGA or CPLD device speed grade and the duty cycle resolution requirements [3].

It was studied and presented that the PLD (FPGA) based digital controllers are far better than Digital Signal Processors based as they have better dynamic performance and control capabilities[4]. In many market segments, such as handheld devices, PLDs have found acceptance due to new product architectures that reduce power consumption, feature new packaging options, lower unit cost and shorter design cycle. Present work describes the design and development of Generic Complex Programmable Device (CPLD) board for various applications explained in preceding paragraphs.

2. HARDWARE DESIGN AND DEVELOPMENT

Over the past few years, the density of the average programmable logic device has begun to skyrocket. As chip densities increased, it was natural for the PLD manufacturers to evolve their products into larger (logically, but not necessarily physically) parts called Complex Programmable Logic Devices (CPLDs). The larger size of a CPLD allows designers to implement either more logic equations or a more complicated design. In fact, these chips are large enough to replace dozens of those pesky 7400-series parts. Present board design uses ALTERA CPLD MAXII series EPM-570T144C5 TQFP144 package to demonstrate the generic nature of the board.

2.1 Features

- On Board DC-DC converters.
- On Board JTAG Interface.
- Compact (4" X 3").
- Low Power consumption.
- Visual indication for power, programming
- On board clock circuitry
- Seven segment display control interface
- LED interface.
- Reverse polarity protection.

2.2 Block diagram

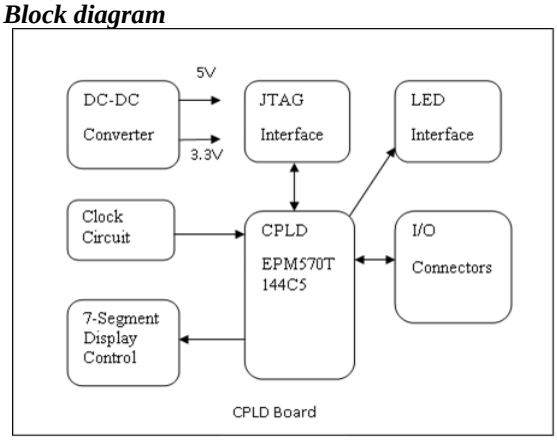

Figure1. Block diagram of CPLD Board

The block diagram of the present work is shown in figure 1. As indicated in thye block diagram it consists of:

i. DC-DC Converters.
ii. JTAG Interface.
iii. LED Interface.
iv. Clock Circuit.
v. CPLD
vi. 7-Segment Display
vii. Input/output Connectors

The developed prototype is shown in figure 2.

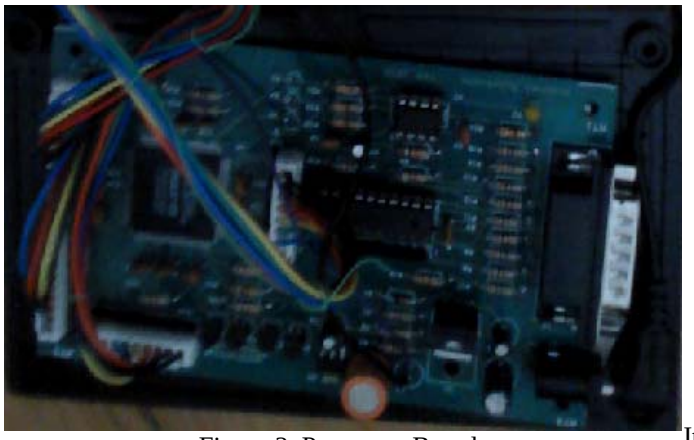

Figure 2. Prototype Board

2.2.1 DC-DC Converters

The popular voltage regulators LM317 and LTC1963-3.3 are used to derive 5V and 3.3 V for the board operation. These are provided on the board. These are used to power up clock, 7-segment display; LED interface and CPLD. Each device can deliver 1.5A.

2.2.2 JTAG Interface

The JTAG interface is realised using regular SN74HC245 device with few passive components on the board to avoid the cable length problem while programming as it interfaces with PC parallel port and the board. Generally such cables are of few centimetres in length. This limitation is over come in this board design. There is a LED indication to indicate the programming activity. The JTAG interface cable is shown in figure 3.

Figure 3. JTAG Cable

2.2.3 LED Interface

These LED interfaces are provided to indicate the presence of the power and any other activity to indicate visually.

2.2.4 Clock Circuit

The clock circuit is realised with a low cost LM555 timer IC with passive components. By varying the values of resistors and capacitors, any required frequency clock can be generated if needed.

2.2.5 CPLD

The selected CPLD is from ALTERA, MAXII series device EPM570T144C5 and 144 pin TQFP package. The block diagram of this CPLD is shown in figure 4.

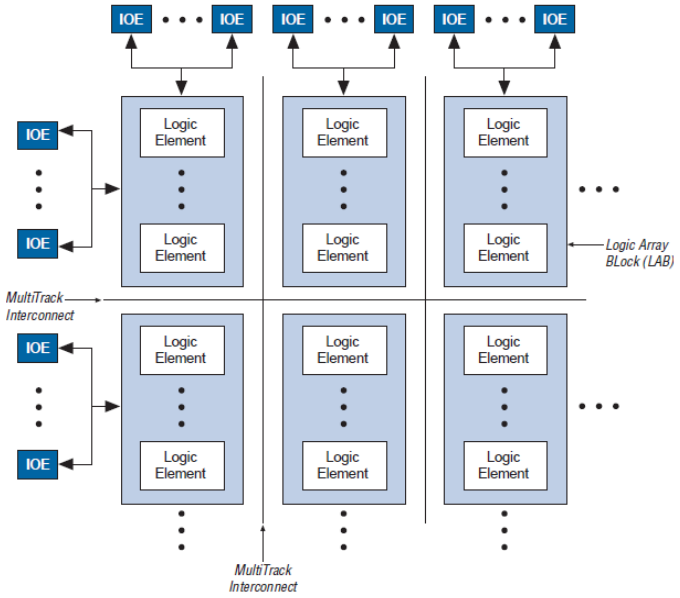

Figure4. Block diagram of CPLD.

It has 570 logic elements (LE) which will be configured based on the design requirements. For medium size digital designs this device is more than sufficient. The structure of the logic element (LE) is shown in figure 5.

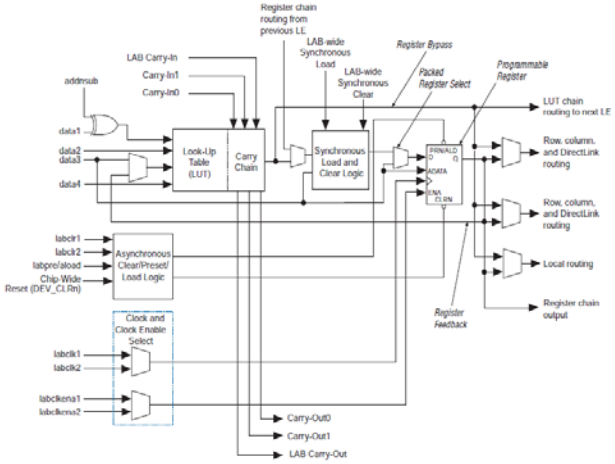

Figure5. LE Structure.

MAX-II devices contain a two-dimensional row- and column-based architecture to implement custom logic. Row and column interconnects provide signal interconnects between the logic array blocks (LABs).The logic array consists of LABs, with 10 logic elements (LEs) in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device. The Multi-Track interconnect provides fast granular timing delays between LABs. The fast routing between Les provides minimum timing delay for added levels of logic versus globally routed interconnect structures. The MAX II device I/O pins are fed by I/O elements (IOE) located at the ends of LAB rows and columns around the periphery of the device. Each IOE contains a bidirectional I/O buffer with several advanced features. I/O pins support Schmitt triggers inputs and various single-ended standards, such as 66-MHz, 32-bit

PCI, and LVTTL. MAX II devices provide a global clock network. The global clock network consists of four global clock lines that drive throughout the entire device, providing clocks for all resources within the device.

2.2.6 Seven-Segment Display

Seven segment display control circuitry is designed using transistors and will sync the current when common anode seven segment display is interfaced. This also allows the designer to use a common data bus to interface multiple segments there by reducing the components count on the board.

2.2.7 Input/output Connectors

These are provided to interface the board to the external world.

3. INTERNAL HARDWARE DESIGN OF CPLD

The Electronic Design Automation (EDA) tool called QUARTUS-II from Altera is used to design the internal hardware of the CPLD. A description of the hardware's structure and behaviour is written in a high-level hardware description language (usually VHDL or Verilog) and that code is then compiled and downloaded prior to execution. Of course, schematic capture is also an option for design entry, but it has become less popular as designs have become more complex and the language-based tools have improved. The overall process of hardware development for programmable logic is shown in Figure 6.

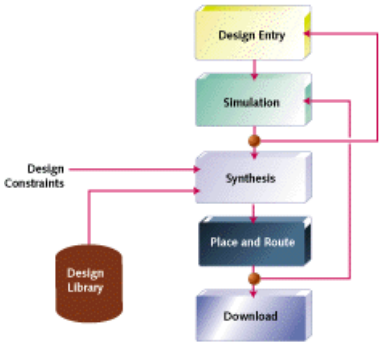

Figure 6. Programmable logic design process

3.1 A5/1 Algorithm

The global system for mobile communications (GSM) is considered as the second generation (2G) mobile phone system and made mobile communications accessible for the mass market. In many industrial countries the number of mobile subscribers even exceeds that of the conventional telephone network. GSM and its underlying security architecture were developed back in the 1980s. Because it is widely deployed and became ubiquitous in most countries around the world it is still growing in coverage.

A5/1 is the stream cipher used to secure over the air communication (GSM). This algorithm provides a reasonable amount of resistance to the attacks. It consists of three linear feedback shift registers (LFSR). The register lengths are 19, 22 and 23. The output is the XOR of the three LFSRs. A5/1 uses a variable clock control. Each register is clocked based on its own middle bit, XORed with the inverse threshold function of the middle bits of all the three registers. Usually, two of the LFSRs clock in each round. The structure of A5/1 is shown in figure 7.

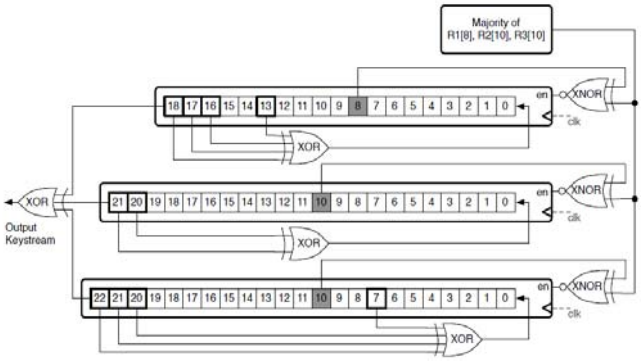

Figure 7. Structure of A5/1 GSM Algorithm

3.2 Seven Segment Display Driver

The structure of the BCD to seven segment decoder is shown in figure 8. This is used to display the encrypted message along with the plain text generated using counter.

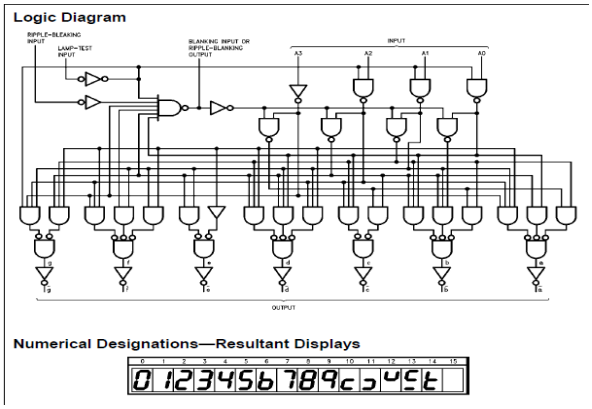

Figure 8. Structure of BCD to Seven Segment Decoder.

3.3 Binary Counter-8 Bit wide

8-Bit binary counter is used to generate the different clock rates for generating pseudorandom bit sequences (PRBS) to encrypt the plain text and also to divide the input clock frequency to the required value.

All these are implemented using high level language VHDL and the top level is with Schematic. VHDL entities of various devices implemented within the CPLD are shown in figure 9.

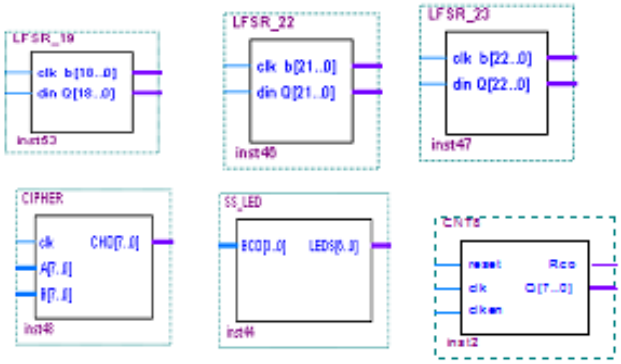

Figure 9. VHDL entities.

The complete implementation and developed prototype is as shown in figure 10a and 10b.

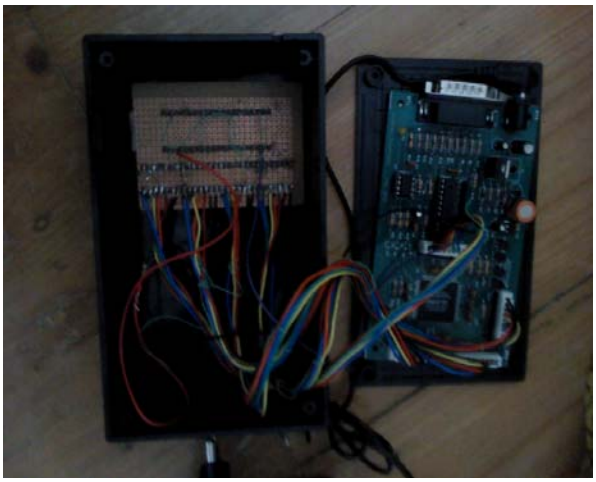

Figure10a. View of the complete prototype.

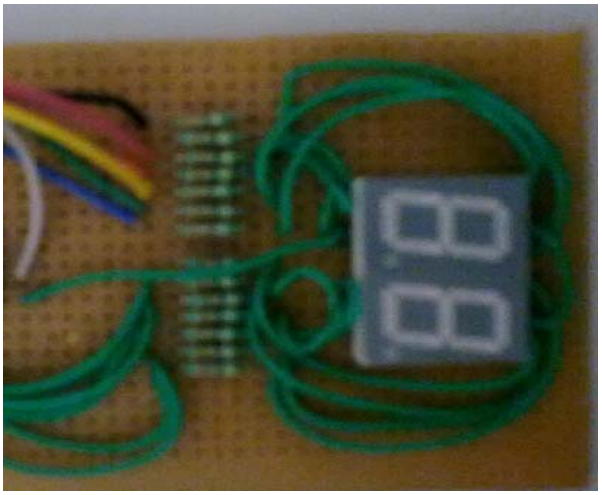

Figure 10b. Seven Segment Display

3.4 Synthesis Report

As discussed in the preceding sections A5/1 algorithm with three LFSRS of size 19, 22,23 and other glue logics have been implemented in VHDL . Even the counters, seven segment display driver have been implemented in VHDL. All these are combined and synthesized the code for CPLD. The same has been tested and confirmed the functionality of those implemented tasks. The synthesis report is shown in Table 1.

Parameters		Utilization %
Total Logic Elements	103/570	18
Total Registers	92/570	16
Total LABs	16/57	28
Total I/Os	35/116	30
Global Clocks	4/4	100

Table 1. Utilization of Resources

4. APPLICATIONS

As detailed in preceding sections this board is generic in nature and it can be utilised for various applications such as:

a. VHDL/Verilog Language trainer kit.
b. It can be used in system designs as add-on module.
c. ASIC design and development.
d. Embedded System designs.
e. Encryption algorithm implementation and verification.
f. Voice compression algorithm implementation.
g. Reconfigurable hardware in various embedded, instrumentation, medical, communication systems.
h.

5. CONCLUSION

In this paper, a generic CPLD board design and development is presented. It has been studied and demonstrated that the designed board is generic in nature and it can be used in various system designs as a reconfigurable hardware in the field of communication, medical electronics, and industrial electronics, VLSI, embedded. Even it can be used as a VHDL/Verilog trainer kit in educational institutions. Size of the board can be still reduced if all SMD components are used. Then the module will be of 2”x3” or even smaller.

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